

# PARALLEL CONNECTED DC-DC BUCK CONVERTER FOR HIGH POWER TRANSFER USING SOFT-SWITCHING

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**Abstract-** In this proposed work buck converter is provided with a high power which is transmitted to the load through a soft-switching topology. The transfer of this high power to the load is possible since the switches are connected in parallel and this prevents the switches from being damaged because of the high current. Without the use of auxiliary switches zero voltage switching and zero current switching is obtained which makes the proposed circuit more simple. All the switches in operation at a time transmit equal power to the load which increases the reliability and efficiency of the switches. There is not only the reduction in input current and output voltage ripple but also results in small size and less cost of the converter circuit due to the use of common soft-switching method. In spite of using four operating switches the control of the converter is simple. Different modes of operation of converter are shown with dc analysis. ZVS and ZCS can be obtained by single switch which reduces switching losses and efficiency is increased.

Comparison of the charging of a battery with ideal source is carried out with the battery connected to the proposed topology and the results obtained in both the cases are similar to each other which are represented by the graphs obtained through the simulation performed in the SIMULINK model of MATLAB. With the proposed converter circuit efficiency of 97% is achieved.

**Keywords:-** Buck Converter, Interleaved, ZVT-ZCT Technique, Resonant Converter, Soft-Switching.

## 1 INTRODUCTION

In the last few decades, with the continuous improvement in power electronics, results not only in the advanced power devices but also gives new convertor control and topologies. With the increase in the rate of the electrical power consumption during these days causes the rise in the usage of the power electronic devices so that the quality of the electrical power is improved and has better control. With the ability to withstand across high switching frequency and in addition with smaller in size and light in weight Switch Mode Power Supply (SMPS) has been taken into account.

In this thesis the work carried out represents the interleaved Buck convertor. The circuit with the topology proposed consists of the two parallel buck convertor with operating time 180° apart to one another. With the characteristics of Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) at the time of turn ON and turn OFF soft switching is used for the main and auxiliary switches in the convertor circuit which is being proposed.

### 1.1 Introduction to Switching

Further switching can be classified into two types based on various parameters such as switching losses, stress among

the switches and the electromagnetic interference;

- Hard Switching
- Soft Switching

At present soft switching has replaced hard switching because of some of its drawbacks. Soft switching can be defined as the switching process in which the device voltage or current is zero when the transition occurs. With the use of soft switching the efficiency of the circuit is increased with the reduction in switching losses which is associated with hard switching used in conventional convertors.

Soft switching is being implemented in this dissertation based on the above possible solution and the work presented in this module makes use of both ZVS and ZCS to achieve soft switching.

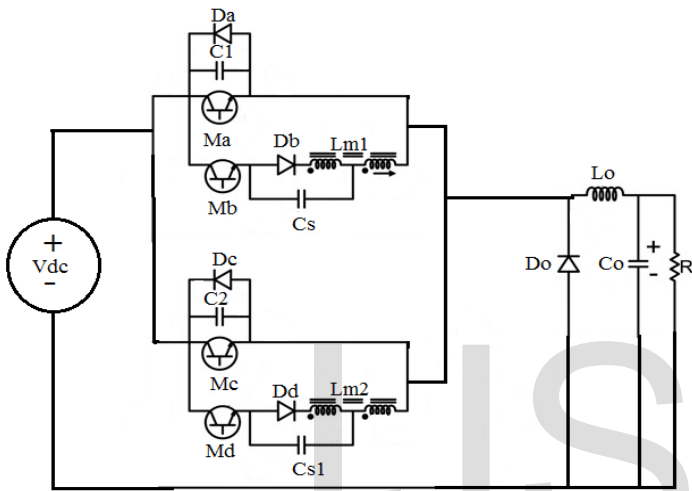
### 1.2 Soft-switched converters

Soft switched convertors can be defined as the convertors which have the advantages of both PWM convertors and resonant convertors. When compared to the resonant convertors resonance is fully utilized in controlled ways in soft switching convertors. In soft switched convertors, just before and during turn ON and turn OFF processes resonance is allowed to occur due to which convertors

behave as conventional PWM converters so that condition of ZVS and ZCS can be achieved. With the use of soft switched converters there is the reduction in the switching losses and stress among the switches and also electromagnetic interference is suppressed by the use of these converters.

## 2 PRINCIPLE OF OPERATION

Under this section, classification of the different modes of operation of the proposed circuit topology is carried out. The focus is to design the converter without galvanic separation and with the use of auxiliary switches.



**Fig 2.1:- The proposed circuit for the interleaved buck converter.**

As shown above the suggested circuit is basically the combination of two buck converters which are connected in parallel to each other also balanced work of operation is achieved because of the interleaved topology. Soft switching used in the above circuit provides the reliable output with increased efficiency since the load is provided with equal amount of power by the switches due to which they are equally stressed. The switches are split in phase by 180° with 0.5 of maximum duty cycle of each switch.

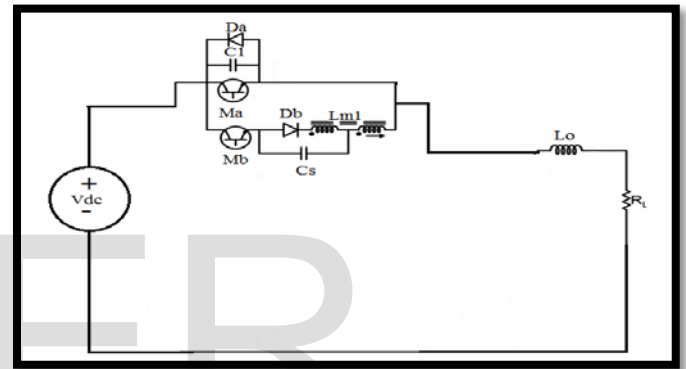
Ma and Mb are provided with one signal and Mc and Md is provided with other signal. The major inductor Lo is equipped with a series connected small commutating inductors Lk1 and Lk2 resulting in lesser stress on the switches. Parasitic inductance is neglected and the MOSFET switches voltage stress is balanced with the input voltage (Vin).

This topology is most suitable for high power range because of more number of operational switches also multiplication of the switches is unavoidable due to increase in power transfer as the converters are connected in parallel. With the parallel connection of switches, soft-switching is also implemented and for operations involving high power this converter is best suited [1].

## 2.1 Different Modes of Operation

There are total 10 modes of operation of this topology according to the switching timing. But since the interleaved converter is being proposed hence only 5 modes are discussed and other 5 modes are exactly similar to the discussed modes. Modes included in this section are from MODE 1 to MODE 5.

**MODE 1:- Conduction of Ma and Mb, [t0 – t1];** The circuit represented in figure 1 is the proposed circuit for operation. The load is provided with the transferred energy from the supply because the circuit during this interval behaves as ordinary hard-switching buck converter. The inductor current simply rises to the value of ILM till the time interval t1. Charging of the commutating capacitor C2 up to the input voltage Vin takes place. Turn-off of Ma and Mb takes place with zero voltage switching at t = t1.

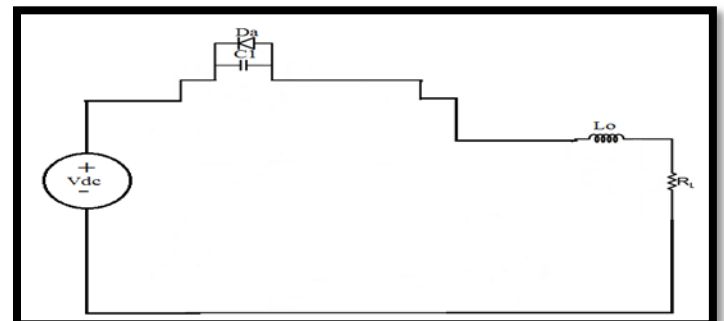


**Fig 2:- Circuit for the operating mode 1.**

t01 is the time interval of this mode which can be written as;

$$t_{01} = T (D_o - 0.5)$$

**MODE 2:- Turn Off interval, [t1 – t2];** Under this mode opening condition of the switches Ma and Mb takes place at the same time. In this mode mainly the diodes Da and Db are in operation. Since switches are not conducting, the inductor current iLo starts flowing through diodes D12, D11 and the capacitor C1. In this mode soft-switching is achieved by ZV turning off the switches. No conduction of the main diode D takes place and the voltage value of Ck1 reaches to input voltage Vin from zero value as the reverse voltage across Do falls from value of Vin to zero.



**Fig 3:- Circuit for operating mode 2.**

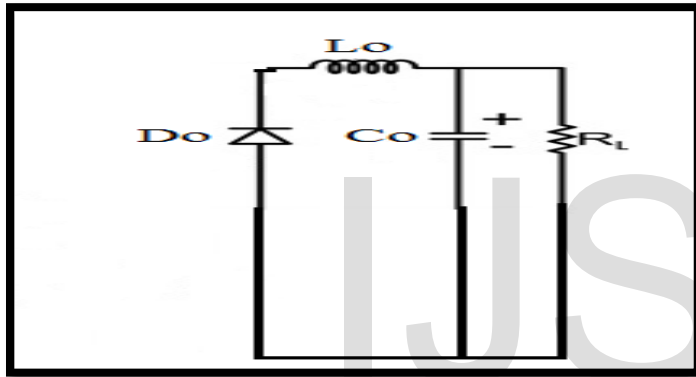
The increase in voltage of  $C_{k1}$  is from  $V_{in}$  to  $\Delta V$ .

Where,

$$\Delta V = I_M \sqrt{\frac{L_{1ek}}{C_K}}$$

During this interval, voltage on the switches  $M_a$ ,  $M_b$  and the capacitor  $C_{k1}$  is similar and the maximum stress of voltage on the MOSFET's is given by  $V_{in} + \Delta V$  which is not shown. The assumption made for the waveforms is  $L_{1ek} = 0$ .

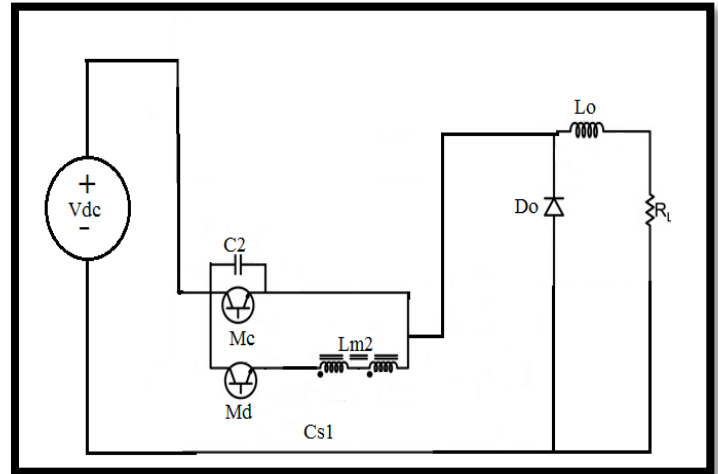
**MODE 3:- Conduction of  $D_o$ ,  $[t_2 - t_3]$ ;** In this mode free-wheeling condition arises. Since no switching pulse is provided to switches due to this all the switches are in off state. The load is supplied with the power by the main diode  $D_o$  as the free-wheeling interval of the diode  $D_o$  results in its conduction.



**Fig 4:- Circuit for the operating mode 3.**

Operation of the proposed circuit during this interval is represented by the figure shown above. With the turning off of the switches free-wheeling of the main diode  $D_o$  takes place. The effect of the parasitic inductance  $L_{1ek}$  is neglected in this time interval.

**MODE 4:- Turn On interval,  $[t_3 - t_4]$ ;** In this interval switching pulse is provided to the switches  $M_c$  and  $M_d$  for their turn on.  $D_2$  attains the value of reverse voltage which is equal to the twice of input voltage  $2V_{in}$  and this shows the maximum voltage stress that can be achieved by the main diodes. In this interval, turn on of the switches is achieved using zero current (ZC).



**Fig 5:- Circuit for the operating mode 4.**

The above figure represents the simplified circuit of mode 4 operation in order to make the calculation for the switch current.

Solution for switch current  $i_{MC} = i_{MD} = i_{S2}$  gives;

$$I_{S2}(t) = 2V_{in} \sqrt{\frac{C_k}{L_m}} \sin \frac{t-t_3}{\sqrt{L_m C_k}}$$

$$\left(\frac{di_{S2}}{dt}\right)_{t=t_3} = \frac{2V_{in}}{L_k}$$

Discharging of the input current stored in the capacitor  $C_2$  takes place at the same instant. The expression for the diode current can be derived as follows;

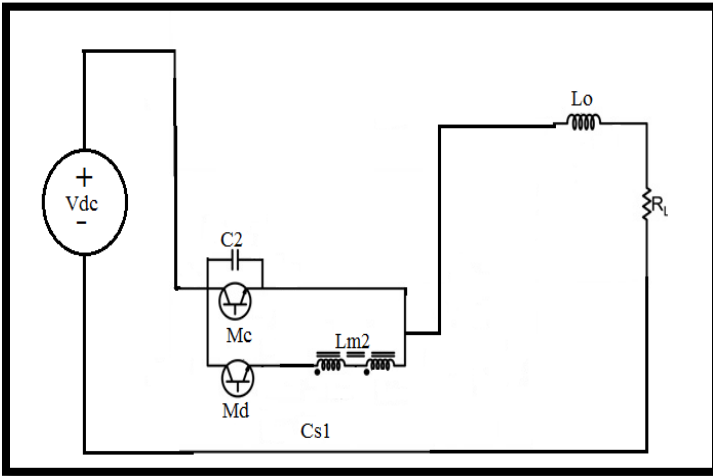
$$I_{D1} = I_m - 2V_{in} \sqrt{\frac{C_k}{L_m}} \sin \frac{t-t_3}{\sqrt{L_m C_k}}$$

The condition coming out of equation (5) is given by;

$$I_m < 2V_{in} \sqrt{\frac{C_k}{L_m}}$$

Capacitor  $C_2$  is not completely discharged if the above shown condition is satisfied and the oscillatory input current results in turning off of the diode. Thus for this reason condition (6) when not satisfied is no longer taken into account.

**MODE 5:- full discharge of  $C_1$ ,  $[t_4 - t_5]$ ;** In this mode of operation, discharging of the capacitor  $C_2$  continues with the approximate value of constant current given by the main inductance  $L_o$ .



**Fig 6:- Circuit for the operating mode 5.**

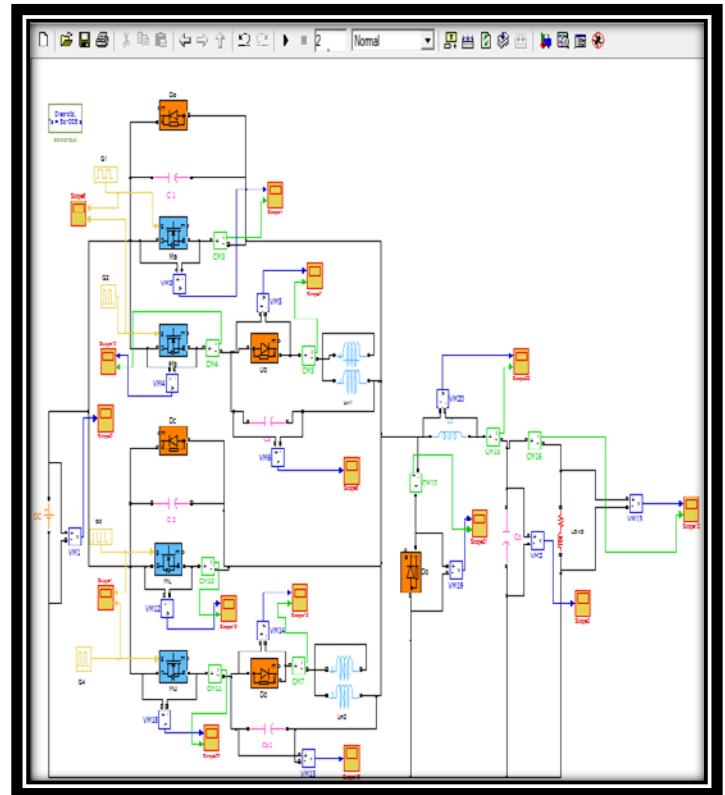
In this interval turning on of the diodes  $D_c$  and  $D_d$  takes place with the complete discharging of the capacitor  $C_2$  resulting in the conduction of other interval with the switches  $M_c$  and  $M_d$ .

### 3 SIMULATION AND RESULTS

This section comprises of the simulation of the topology which is being proposed for the circuit in addition with its various output waveforms. The simulation of the circuit is performed in SIMULINK which is the section of MATLABM software.

#### 3.1 Proposed Simulated Circuit Configuration

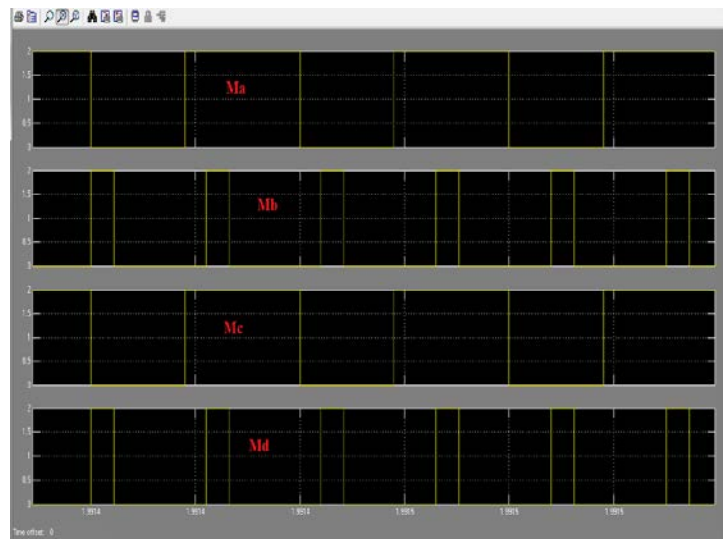
The figure shown below represents the simulation circuit of the proposed topology.



**Fig 7:- Simulated circuit of the proposed interleaved buck converter.**

While simulating the proposed circuit we assume that all the switches we are taking are ideal in nature. The switches and the line connecting across the switches are loss free. While selecting the inductor we assume that it does not have any resistance in it.

#### 3.2 Gate Pulse to the MOSFETs



**Fig 8:- Gate pulse provided to the switches  $M_a$ ,  $M_b$ ,  $M_c$  and  $M_d$  of the converter.**

### 3.3 Load Voltage and Current

Graphs of load voltage and current are obtained as shown below when the dc source of 150 volts is applied at the input of the converter.

#### 3.3.1 Load Voltage

The input of converter is fed with 150 V dc supply. The load taken at the output of the converter circuit is of RL type. The voltage obtained at the load end is 91 V and this satisfies the ratio of duty cycle of the proposed topology for the converter.



Fig 9:- Load or output voltage.

As the output obtained does not contain any ripple, this shows the effectiveness of proposed topology. Below eq. gives the duty cycle of the converter;

$$D = \frac{V_o}{V_{in}}$$

$$D = \frac{91}{150} = 0.61 = 61\% > 50\%$$

#### 3.3.2 Load Current

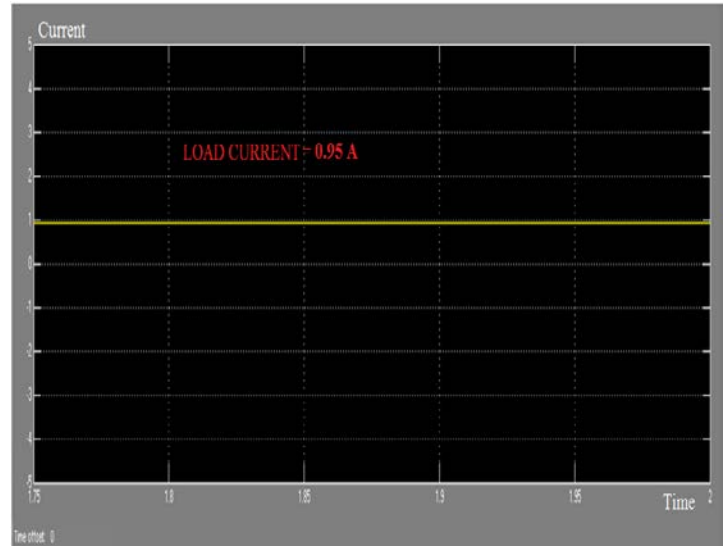


Fig 10:- Load current.

The figure shown above gives the current flowing through the load whose approximate value is 0.95 A when the dc voltage fed to input of the converter is 150 V. Also the ripple free output which we obtained from the above shown figure represents the effectiveness of the circuit used in this topology.

#### 3.4 Switch M<sub>a</sub> switching characteristics

The input of the switch M<sub>a</sub> is provided with a pulse generator which is operating at a switching frequency of 100 kHz and the voltage fed to the input of circuit through a dc source is 150 V.



Fig 11:- Switching characteristics of main switch M<sub>a</sub>.

In the above graph switching of the switch M<sub>a</sub> takes place through Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). ZVS is achieved during turn-on and ZCS is achieved during turn-off.

When the value of voltage is brought to zero or is minimum across the switch ZVS is achieved and at that instant current flow is maximum. And ZCS condition is achieved with zero current and maximum voltage across the switch and thus with switching-off of the switch characteristics are achieved.

### 3.5 Auxiliary Switch $M_b$ switching characteristics

Switch  $M_b$  is directly fed from the 150 V dc supply. The input of the switch  $M_b$  is provided with a pulse generator with its switching frequency and the voltage fed to the input of circuit through a dc source is 150 V.

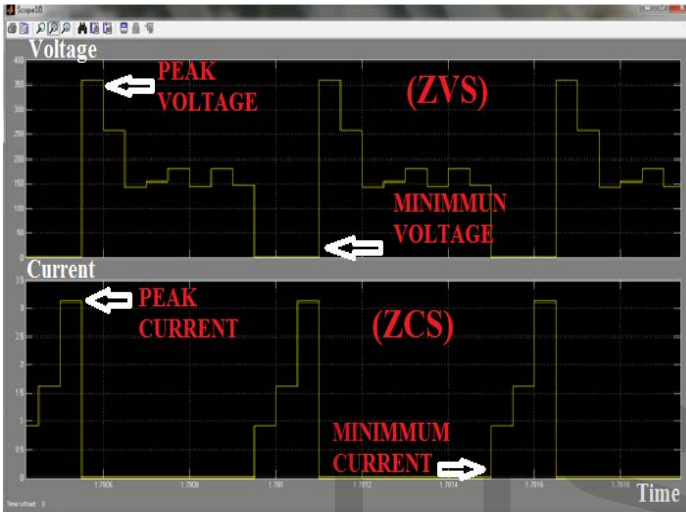


Fig 12:- Switching characteristics of auxiliary switch  $M_b$ .

The above figure shows ZVS and ZCS achieved for the switch  $M_b$  at the time of turn-on and turn-off.

The stress on this switch is high and the properties of this switch are different from that of the man switch  $M_a$ . ZVS condition is obtained when the voltage across the switch is brought to zero or is minimum with maximum current across it. ZCS condition is obtained with zero current and maximum voltage across the switch and thus with switching-off of the switch characteristics are achieved.

### 3.6 Switch $M_c$ switching characteristics

The input of the switch  $M_c$  is provided with a pulse generator which is operating at a switching frequency of 100 kHz and the voltage fed to the input of circuit through a dc source is 150 V.

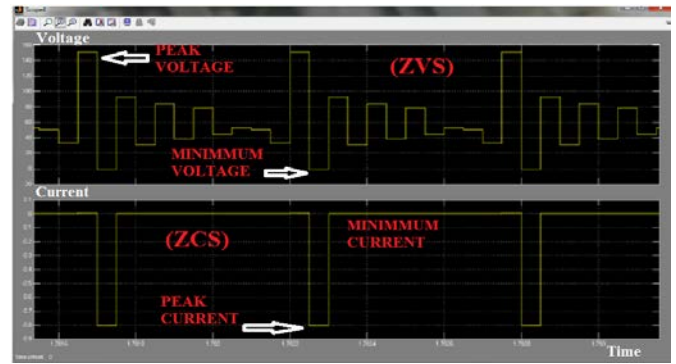


Fig 13:- Switching characteristics of main switch  $M_c$ .

In the above graph switching of the switch  $M_c$  takes place through Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). ZVS is achieved during turn-on and ZCS is achieved during turn-off.

When the value of voltage is brought to zero or is minimum across the switch ZVS is achieved and at that instant current flow is maximum. And ZCS condition is achieved with zero current and maximum voltage across the switch and thus with switching-off of the switch characteristics are achieved.

### 3.7 Output Capacitor ( $C_o$ ) Characteristics

For the proposed topology the connection of the output capacitor is made across the convertor circuit. This capacitor is in parallel with the load and can also be used as the filter capacitor for reducing the harmonics in the output.

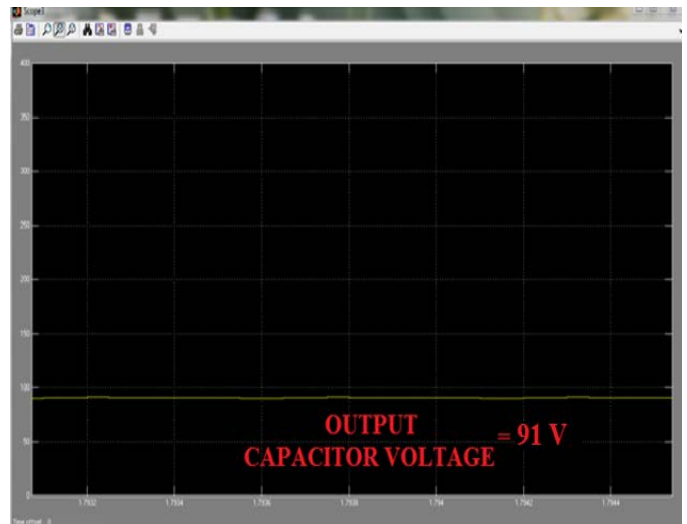


Fig 14:- Output capacitor voltage.

As the output capacitor is connected in parallel with the load due to this reason it has same voltage as that of the load. This capacitor has the capacitance value of and voltage value of Also the output voltage waveform obtained from this capacitor is similar to that of load.

#### 4 Duty Cycle for different Input voltage

Constant duty cycle is obtained when different input voltages are applied at the input of the converter which is shown below;

**Table 1:- Table for the output voltage for different input voltages with constant duty cycle.**

S. No.	INPUT VOLTAGE ( $v_i$ ) (in Volts)	OUTPUT VOLTAGE ( $v_o$ ) (in Volts)	DUTY CYCLE (d) $d = \frac{v_o}{v_i}$
1.	120	74	0.61
2.	130	80	0.61
3.	140	86	0.61
4.	150	91	0.61
5.	160	98	0.61
6.	170	105	0.61
7.	180	110	0.61

The duty cycle with these variations in voltage has been calculated and the results we achieve are constant in nature. Thus, this shows the effectiveness of the proposed circuit topology.

#### 5 Operation of converter for different duty cycle

Operation of converter for different duty cycles is also carried out and following results are obtained;

**Table 3:- Performance of converter for different duty cycles.**

S. No.	Input Voltage ( $v_i$ )	Output Voltage ( $v_o$ ) (d = 0.61)	Output Voltage ( $v_o$ ) (d = 0.71)	Output Voltage ( $v_o$ ) (d = 0.82)
1.	120	74	85	98
2.	140	86	100	115
3.	160	98	114	130
4.	180	110	129	148

It is clear that the converter is performing the buck operation for different input voltages. This shows the effectiveness of the proposed circuit with different duty cycle which are greater than 0.5.

#### CONCLUSION

As the proposed circuit is a interleaved buck converter and is stepping down the voltage keeping that the output power in expected range shows the effectiveness of the circuit. The switches of the circuit achieve the soft switching

which gives result in low switching loss. As the switching loss decreases the overall losses of the converter declines and hence the power at the output terminal can be received properly.

The converter topology is best suited for the application of battery charging as the voltage and current are obtained in permissible limit. . The requirement of converters in railways for charging battery can be fulfilled by the use of this converter. The simulation result with its graph shows accuracy as it is simulated in most accurate software called MATLAB.

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